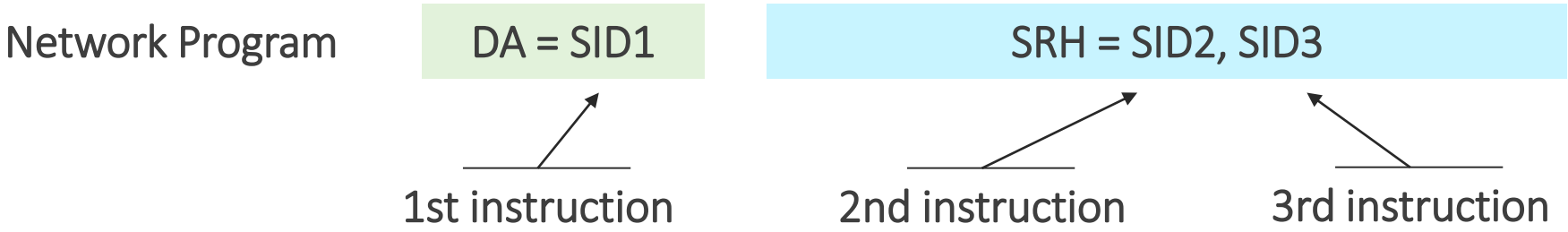
Micro-Program

A new set of (micro)-instructions

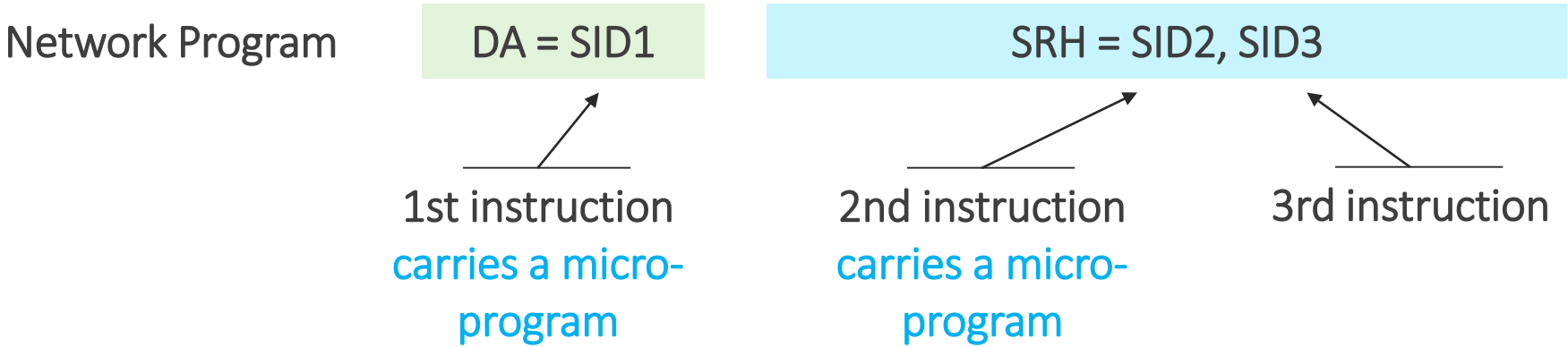
- Full leverage of SRH encapsulation
  - Zero extension
- Full leverage of SRv6 control-plane
  - Zero extension

Network Program

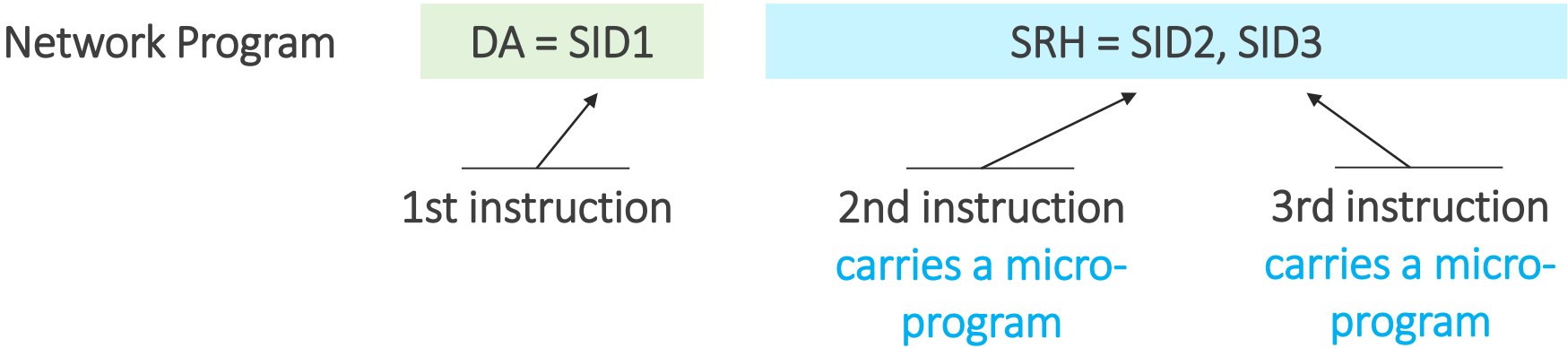


- A network program is a list of instructions (128-bit SRv6 SID)
- An instruction can be bound to any behavior
  - TE/FRR: END, END.X
  - VPN: END.DX, END.DT

Any instruction could hold a micro-program



Any instruction could hold a micro-program



Micro-Program in an SRv6 SID

SRv6 SID = 128 bits = 8 groups of 4 nibbles

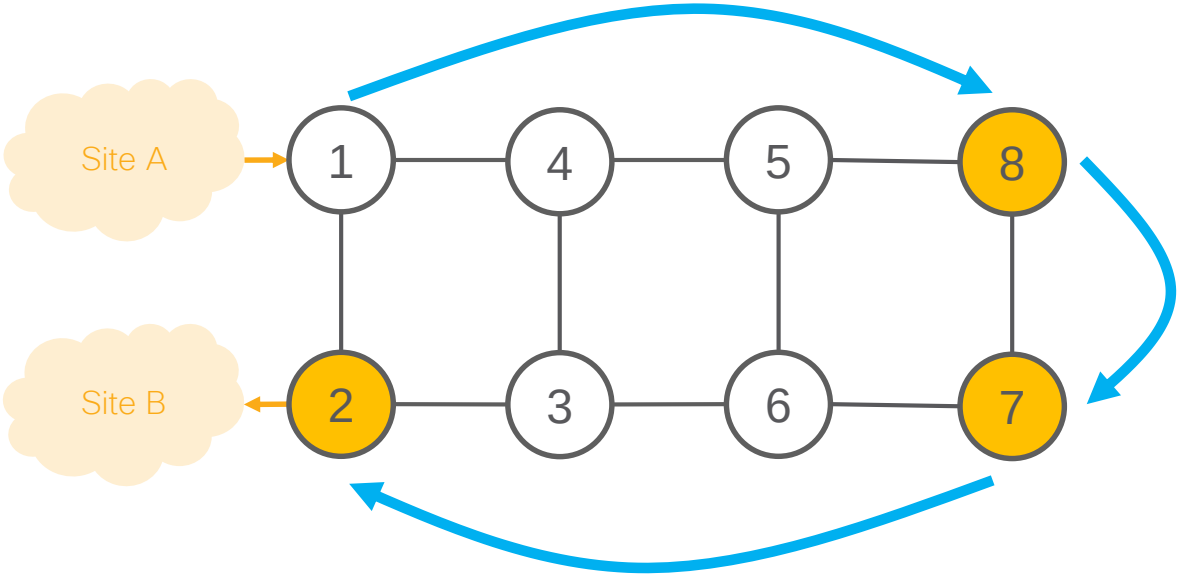
Assuming an allocation block in /32 (B:B::/32)

Assuming a micro-instruction ID in 4 nibbles

B:B:uID1:uID2:uID3:uID4:uID5:uID6

6 micro instructions per SRv6 Instruction

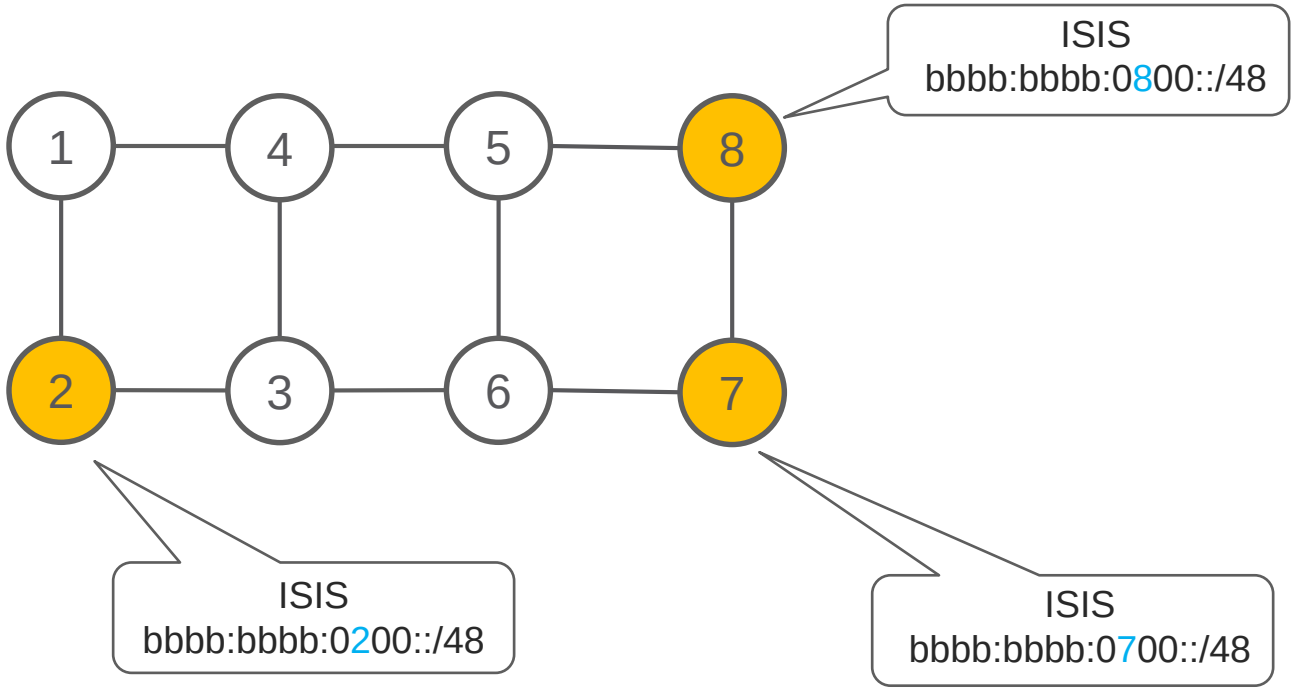
Illustration: go to 8 then 7 then 2 and decaps



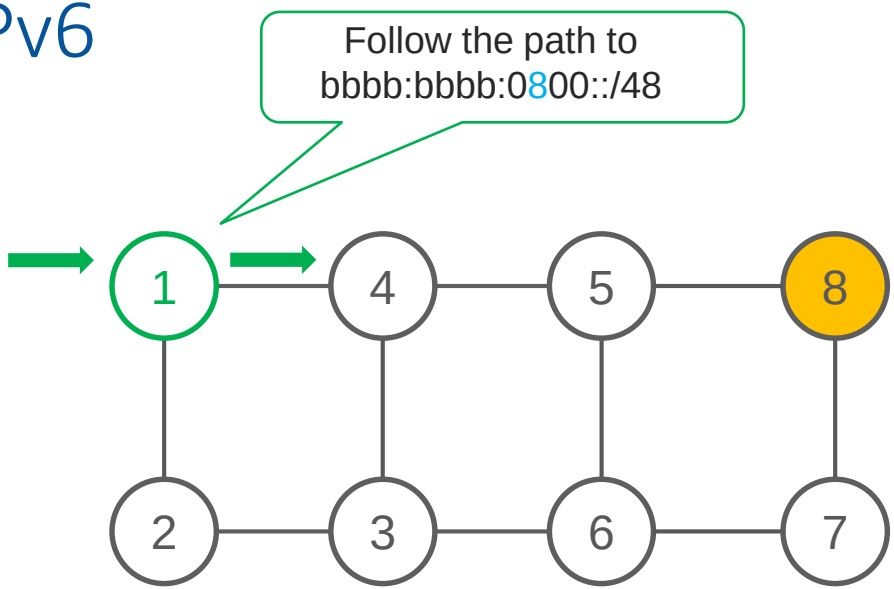
One single micro-program in the DA is enough

DA = bbbb:bbbb:0800:0700:0200:0000:0000:0000

Basic IP Routing: no new extension

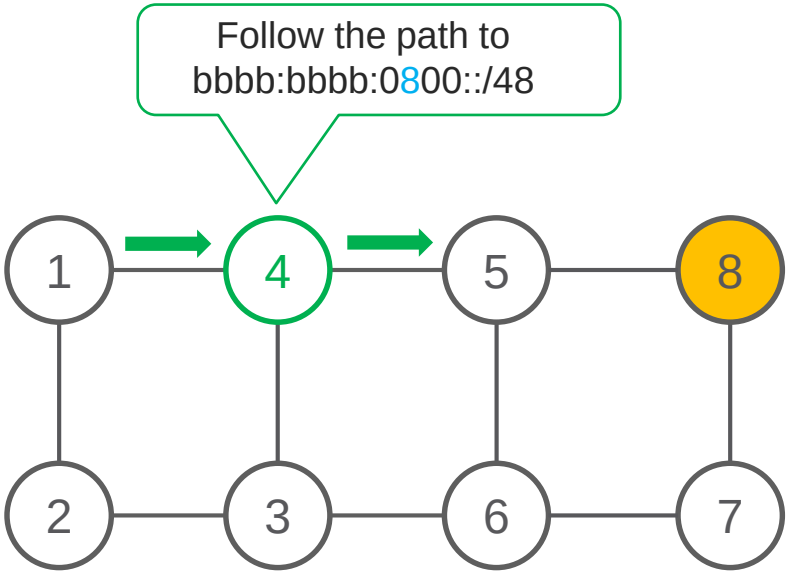


@1: basic IPv6



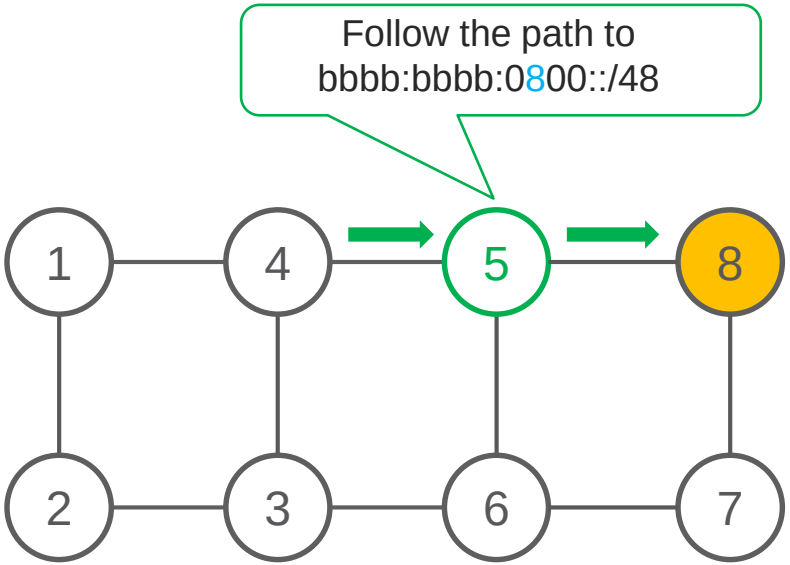
DA = bbbb:bbbb:0800:0700:0200:0000:0000:0000

@4: basic IPv6



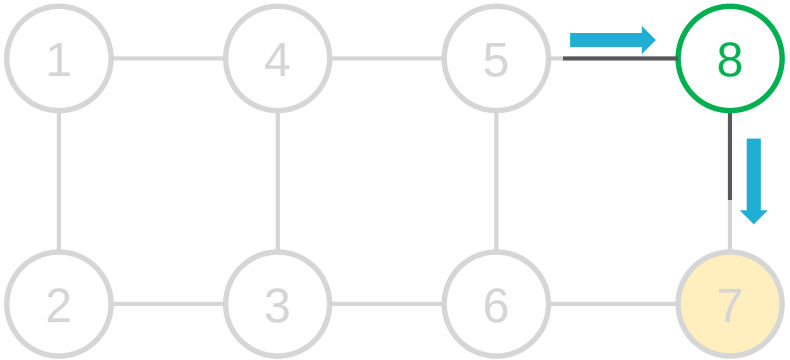
DA = bbbb:bbbb:0800:0700:0200:0000:0000:0000

@5: basic IPv6



DA = bbbb:bbbb:0800:0700:0200:0000:0000:0000

@8: Shift and Forward



Rx'd DA: bbbb:bbbb:0800:0700:0200:0000:0000:0000

SHIFT << 16

Tx'd DA: bbbb:bbbb:0700:

bbbb:bbbb:0700::/48

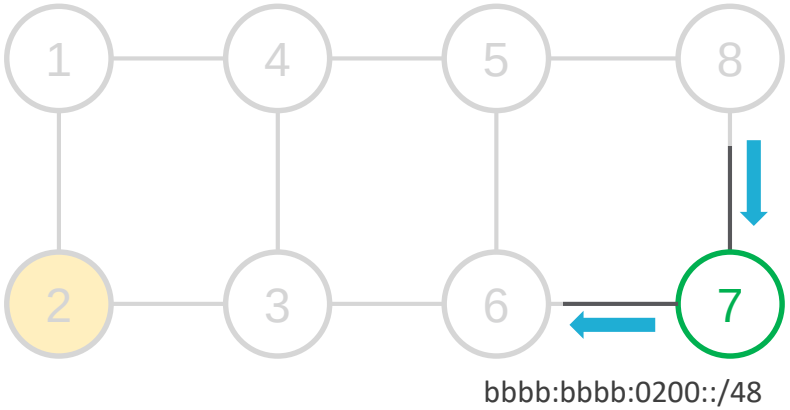
FIB Longest-Match bbbb:bbbb:0800::/48 → SRv6 Instruction:

Shift micro-Program by one micro-Instruction

Set last micro-instruction to "end of micro-program"

Lookup the updated DA and forward

@7: Shift and Forward



Rx'd DA: bbbb:bbbb:0700:0200:0000:0000:0000:0000

SHIFT << 16

Tx'd DA: bbbb:bbbb:0200:

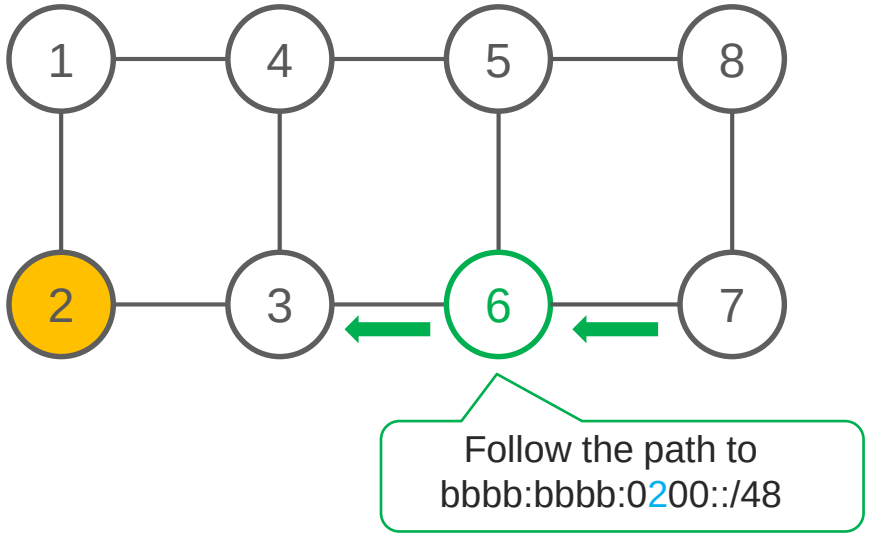
FIB Longest-Match bbbb:bbbb:0700::/48 → SRv6 Instruction:

Shift micro-Program by one micro-Instruction

Set last micro-instruction to "end of micro-program"

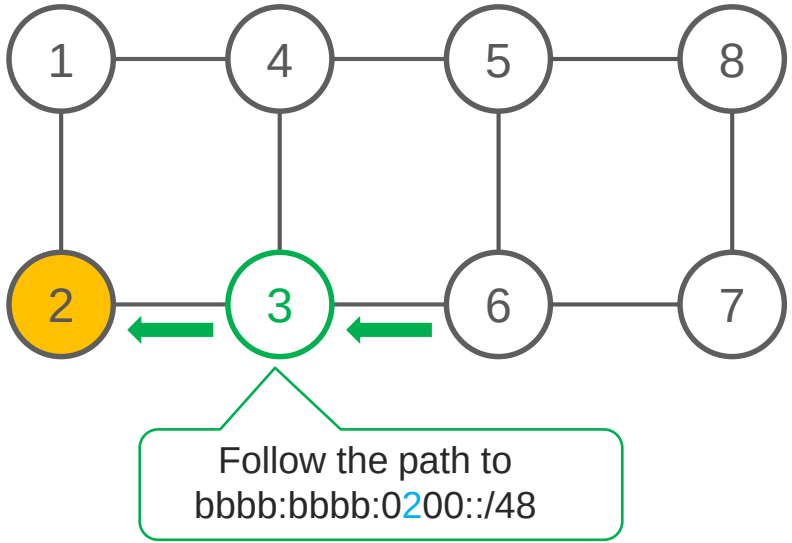
Lookup the updated DA and forward

@6: basic IPv6



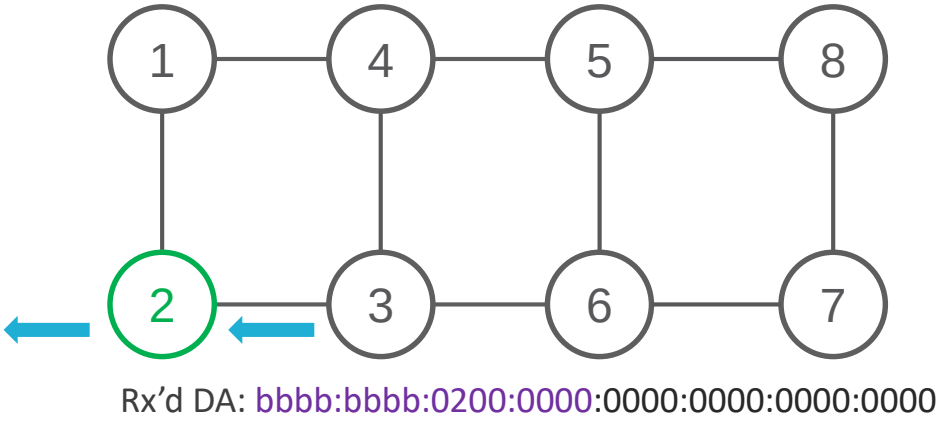
DA = bbbb:bbbb:0200:0000:0000:0000:0000:0000

@3: basic IPv6



DA = bbbb:bbbb:0200:0000:0000:0000:0000:0000

@2: SRv6 End.DX4 behavior



FIB Longest-Match bbbb:bbbb:0200:0000::/64 → SRv6 Instruction:

Decapsulate and cross-connect inner IPv4 packet to Site B

Benefits

- Ultra-scalable for 5G deployment
  - 18 FRR, TE, NFV and VPN micro-instructions in only 40 byte SRH overhead
- Mathematically the best SRv6 compression solution
- Linerate for multi-Tbps hardware
  - Shift is a basic hardware logic
- Friendly to merchant silicon
  - Proven by endorsement and interop
- Friendly to legacy equipment

No Cost

- Full leverage (zero change) to SRv6
  - Net PGM model
  - SRH encapsulation
  - Control Plane
- Seamless Deployment on IPv6 host

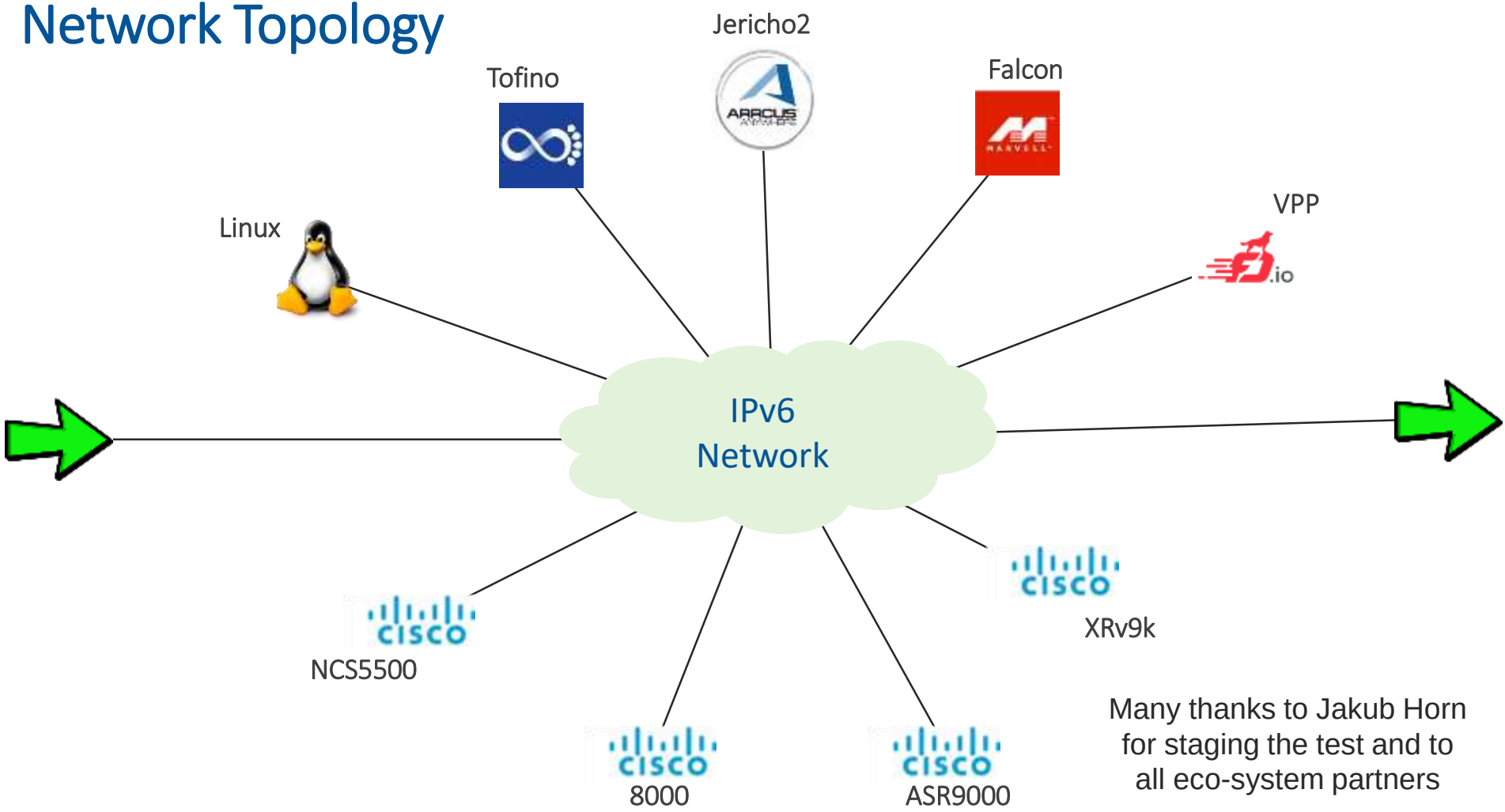
Alibaba

- Dennis Cai reports successful milestone in January 2020
  - SRv6 micro-program linerate hardware verification in Cisco lab
  - Cisco 8000 series (silicon one), NCS-5500, ASR9k
- Use-case
  - Applications are already IPv6 enabled
  - Network is already IPv6-enabled
  - Seamless end-to-end SDN control from Apps through DC, Metro, Backbone

Bell Canada

- Dan Voyer reports successful milestone in January 2020
  - SRv6 micro-program linerate hardware verification
  - Cisco 8000 series (silicon one), NCS-5500, ASR9k, CRS-X
- Use-case: 5G with
  - Ultra Scale
  - Protocol simplification and IPv6 convergence
  - Integrated TE, FRR, Slicing, VPN and NFV for end-to-end value-added service
  - Optimum Load-Balancing
  - Legacy reuse, CRS-X

Network Topology



Many thanks to Jakub Horn for staging the test and to all eco-system partners